A low-frequency ultra-low distortion oscillator

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A low-distortion oscillator is necessary for testing today's ADCs (analog-to-digital converters) that have resolution higher than 20 bits. High-resolution sigma delta AD converters for seismic applications with sampling rates several hundreds samples/s need for testing low frequency signal. An ultra-low distortion oscillator described in (Ref 1) can be easily modified to work in range 100 Hz to 20 kHz but at lower frequencies, two main problems appear: 1. Availability of high quality capacitors with higher values up to 1 uF. 2. A time constant of the AGC loop becomes too long for efficient attenuation of ripple from the rectifier. This article describes the solving of both problems.

The first problem with difficult availability of the high value capacitors is significant especially for film foil polypropylene capacitors because the largest available values are in range 100nF-200nF with size 30 mm x 15 mm so using 5 or 10 of them in parallel is very impractical. Fortunately the second best choice - NPO capacitors - are now available in SMD 1206 case with value 100 nF so stacking 5 pieces and making 0.5 uF in 1206 footprint is possible.

The second problem with the filtering of the ripple voltage from the rectifier is more serious. Only the first order low pass filter can be used because higher order filters make the AGC loop unstable. The sufficient filtering by the first order filter dictates the filter time constant in range hundreds of seconds. This is unacceptable, so different approach has to be used. The solution is using a synchronous filter (Ref. 2.) with theoretically infinite attenuation at switching frequency and the settling time close to one clock cycle.

The resulting circuit is in Figure 1. Frequency of the oscillator is 9.5 Hz with specified values of components. This frequency was chosen because higher harmonics will be easily distinguished from 50/60 Hz interference from mains. IC_9 creates a square wave signal necessary for driving the synchronous filter. The synchronous filter filters an output of the rectifier and consists of IC_6 and IC_8. A time constant of the filter is set by a parallel combination of R_4, R_{14} and C_{23} and should be the same as the oscillator period.

Verification of the oscillator was done again by a combination of a notch filter and FFT analysis of the residual signal from the notch as described in (Ref 1). The notch filter's tuning capacitors and resistors have the same values as in the oscillator. The measured spectrum is in Fig. 2. The output voltage of the oscillator is 10 V_{PP}, = 3.5 V_{RMS} = +10dBV. The second harmonic is -138 dBV, so the second harmonic is 10 dB+138 dB –9 dB = 139 dB below the fundamental. The third harmonic is 10 dB +132 dB –5 dB = 137 dB below the fundamental. The Fig. 1 also shows interference from mains at 50 Hz. It is mainly due to no shielding of the notch filter, which is quite sensitive to interference. If it is a problem some shielding box would be necessary and is highly recommended.

References:

1. Janásek, Vojtěch, "An ultra low distortion oscillator with THD below -140 dB", http://www.janascard.cz/PDF/An%20ultra%20low%20distortion%20oscillator%20with%20THD%20below%20-140%20dB.pdf

2. Woodward, Stephen, "Fast-settling synchronous-PWM-DAC filter has almost no ripple", http://www.edn.com/design/analog/4323340/Fast-settling-synchronous-PWM-DAC-filter-has-almost-no-ripple

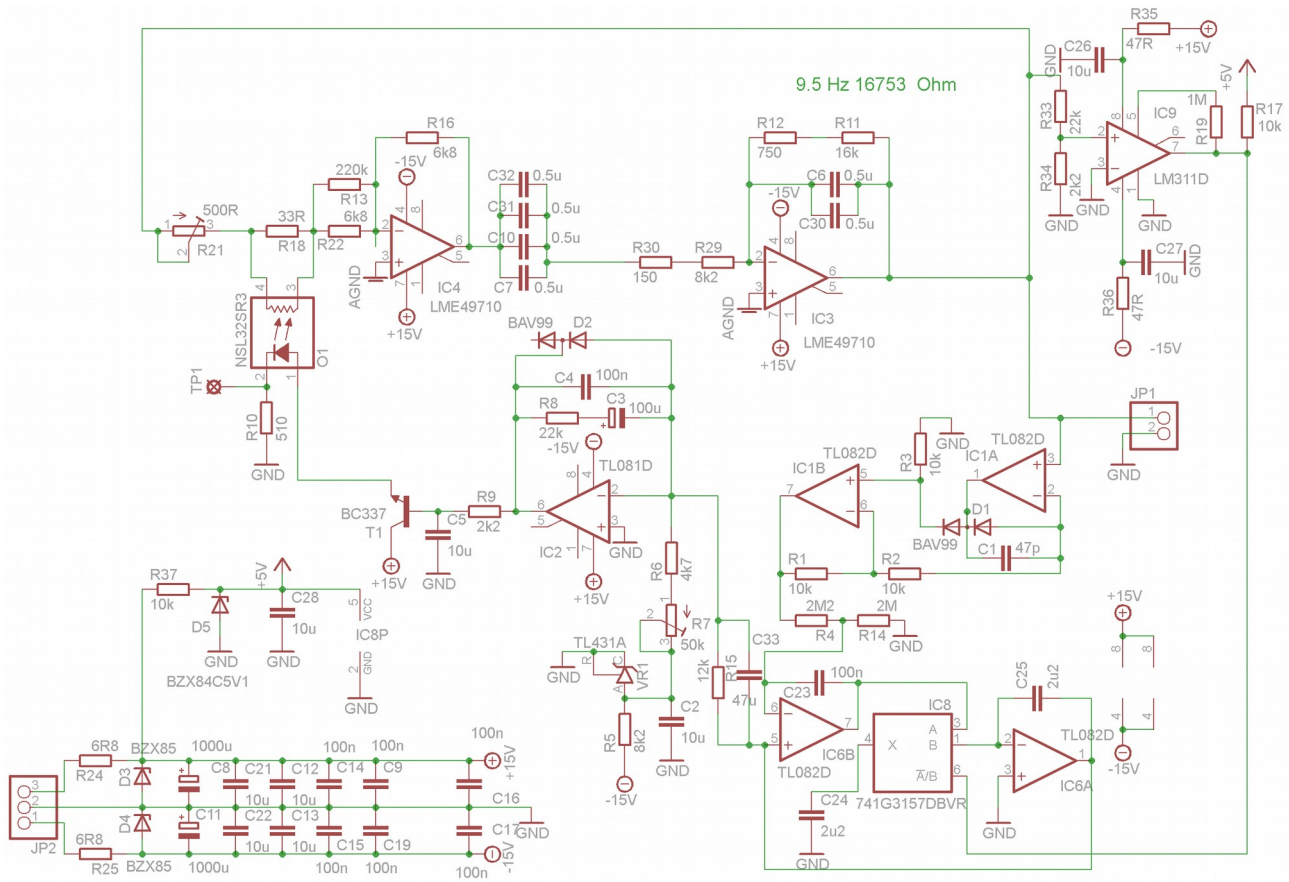

Fig. 1 Ultra-low distortion 9.5 Hz oscillator

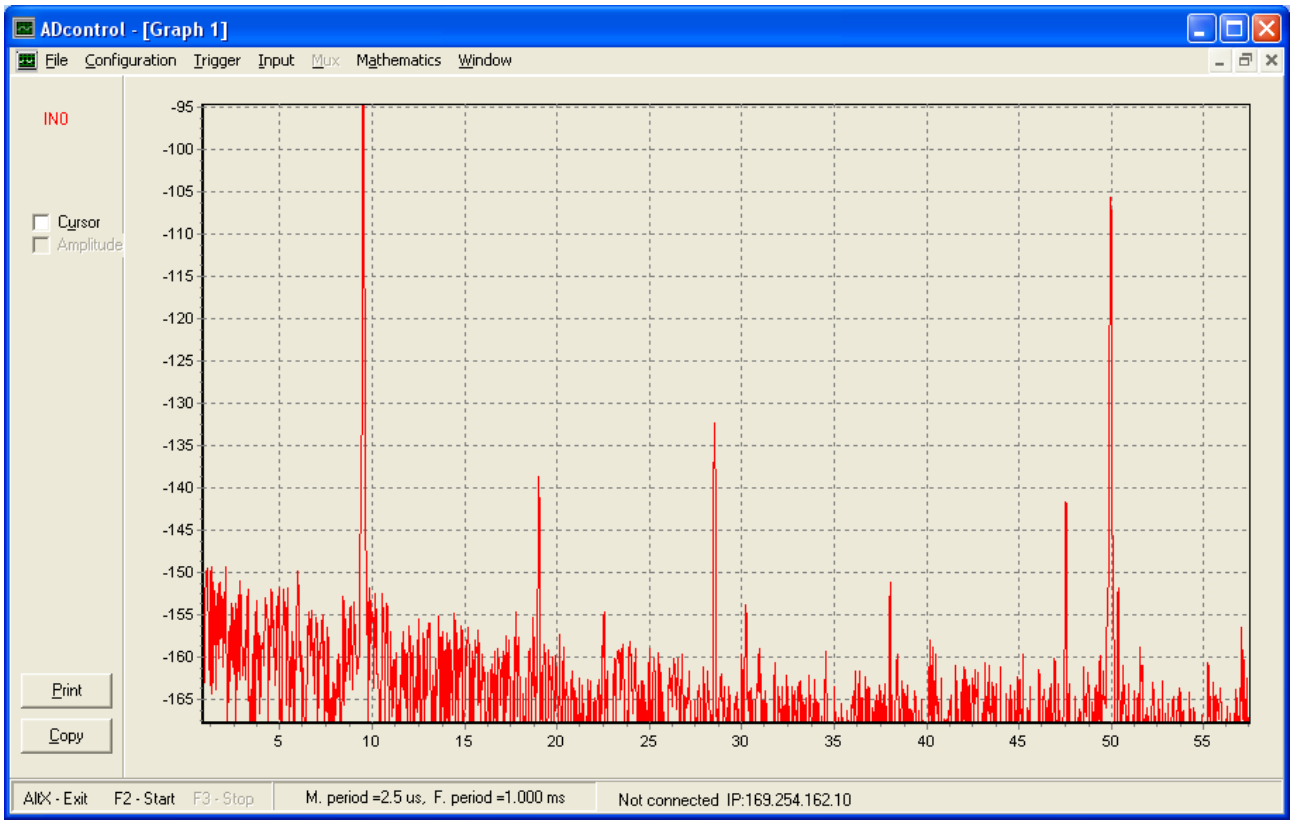

Fig. 2. Spectrum on the output of the notch filter